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Scientific Officer
Solid State Electronics Division
Office of Naval Research
800 North Quincy Street
Arlington, VA 22217-5000

Attention: Mr. Max Yoder, Code 1114SS

Reference: Contract No. N00014-87-C-0314
Item No. 0002, Sequence No. A001
Progress Report No. 11, 1 April 1988 - 30 April 1988

• Baseline HBT Process Development

The first new ADC lot has completed processing and has been shipped to Hughes for evaluation. This lot was processed on a hot lot status to complete it prior to the DARPA review. We made several compromises during the process to expedite the lot, knowing full well that these compromises could jeopardize the functionality of the chips. While the hot lot status did result in the lot being completed prior to the review, only partially functional S/H circuits were obtained, as described below. The major problem associated with this lot was low transistor current gains. Two follow-up lots being processed slightly behind this lead lot also exhibit low current gains. These two lots will be completed during May and shipped to Hughes for evaluation.

Efforts are now focused on solving the low current gain problems. These low current gains are associated with low V_{be} s and are believed to be associated with the ohmic metal contacts. We have begun work to isolate the sources for the excess base currents and special test lots are under way for this function. In addition to these special test lots, ADC lots are being processed so that they will be at the appropriate process steps to quickly implement the improvements as they become available.

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- Circuit Design/Testing Progress

In April, the test software required for wafer-level probing of the S/H circuits was completed. Test software for the 5-bit ADC was completed in the previous month. Hughes received five 5-bit ADC test bar wafers from TI mid-month. Wafer-level probing of the 5-bit ADC and S/H circuits was subsequently completed. No functional 5-bit ADCs were found. However, several partially functional S/H circuits were identified. Wafer-level dc testing indicates the S/H circuits exhibit large dc offsets and degraded gain characteristics. A number of processing factors including extremely low beta, low collector-emitter breakdown voltage, and poor contact and metallization quality contributed to the low yield and poor performance. Therefore, design verification of the 5-bit ADC chip could not be performed with the April lot.

Also this month, fabrication of a custom thin-film hybrid required to dynamically test the 5-bit ADC and S/H circuits was completed. In addition, a dynamic test fixture that supports the custom hybrid was designed and fabricated. All the elements required for complete evaluation of the test-bar chips, from wafer-level probe to high-frequency dynamic test, are in place at this time. Lastly, a detailed architecture study for the 1.5 Gsps 8-bit ADC design was initiated this month.

- Device Characterization

Detailed modeling of the latest 5-bit ADC test-bar devices is not planned due to the poor dc characteristics of the lot. Modeling efforts will be postponed until a more representative overgrowth lot is received.

- Personnel Assignments

There have been no changes in personnel.

- Plans

TI will:

- (1) Run special test to isolate low current gain problems.
- (2) Continue electrically characterizing the completed lots.
- (3) Continue Overgrowth Process Development.

Hughes will:

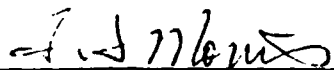
- (1) Complete wafer-level characterization of differential pair V_{be} matching on the April 5-bit ADC test-bar lot.
- (2) Dynamically evaluate the partially functional S/H circuits on the April test-bar lot.
- (3) Complete wafer-level testing of the second test-bar lot expected from TI at the end of the month and verify 5-bit ADC design.
- (4) Dynamically evaluate functional 5-bit ADC and S/H circuits from the May lot.
- (5) Continue architecture study of the 8-bit ADC.
- (6) Initiate detailed characterization of HBT devices from May lot.

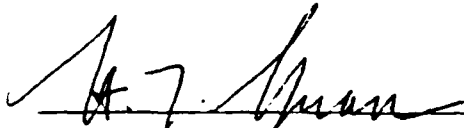
• Unofficial DARPA Financial Status Report


This is the financial status as of 31 March 1988:

| <u>Funds</u> | <u>Funds</u> | <u>Amount</u> | <u>Amount</u> |
|-------------------|--------------|---------------|-----------------|
| <u>Authorized</u> | <u>Spent</u> | <u>Billed</u> | <u>Received</u> |
| FY88 \$1,330,000 | \$941,466 | \$866,467 | \$795,579 |

Contract Number: N00014-87-C-0314
Contract Title: GaAs Heterojunction Device Based A/D
Start Date: 03/30/87


F. J. MORRIS, Principal Investigator
System Components Laboratory


H. T. YUAN, Manager
GaAs Logic and Memory Branch
System Components Laboratory


W. R. WISSEMAN, Associate Director
System Components Laboratory

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